UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,560,958 B1
APPLICATION NO. : 10/619169
DATED : July 14, 2009
INVENTOR(S) : Francisco Javier Guerrero Mercado

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete the title page and substitute therefore the attached title page showing the corrected number of Drawing Sheets in patent.

Delete Drawing Sheets 1-4 and substitute therefore the attached Drawing Sheets 1-2.

Signed and Sealed this

Twenty-second Day of June, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Guerrero Mercado

(10) **Patent No.: US 7,560,958 B1**
(45) **Date of Patent: Jul. 14, 2009**

(54) **LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY**

(75) Inventor: **Francisco Javier Guerrero Mercado**, Landsberg am Lech (DE)

(73) Assignee: **National Semiconductor Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1066 days.

(21) Appl. No.: **10/619,169**

(22) Filed: **Jul. 14, 2003**

(51) **Int. Cl.**
H03K 5/22 (2006.01)

(52) **U.S. Cl.** **327/58**; 327/63; 327/65; 327/89

(58) **Field of Classification Search** 327/52, 327/53, 54, 56, 58, 63, 65, 66, 67, 72, 77–79, 327/80, 81, 88, 89
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,563,533 A 10/1996 Cave et al. 327/67
5,708,673 A * 1/1998 Ikeuchi 372/29.01
5,841,306 A * 11/1998 Lim 327/228
6,051,999 A * 4/2000 To et al. 327/66
6,064,240 A * 5/2000 Wachter 29/407.08
6,323,695 B1 * 11/2001 Heinrich 327/89
6,583,667 B1 * 6/2003 Dasgupta et al. 330/254
6,617,926 B2 * 9/2003 Casper et al. 330/258
6,617,938 B1 * 9/2003 Komiak 332/115
2001/0013851 A1 * 8/2001 Hashimoto et al. 345/91
2002/0190885 A1 * 12/2002 Lin 341/144
2003/0034841 A1 * 2/2003 Fujimura et al. 330/254
2003/0038677 A1 * 2/2003 Teramoto et al. 330/254
2004/0164802 A1 * 8/2004 Hughes 330/261

OTHER PUBLICATIONS

Sedra et al. "Microelectronic Circuits", 1989, pp. 220-223, 337-347.*

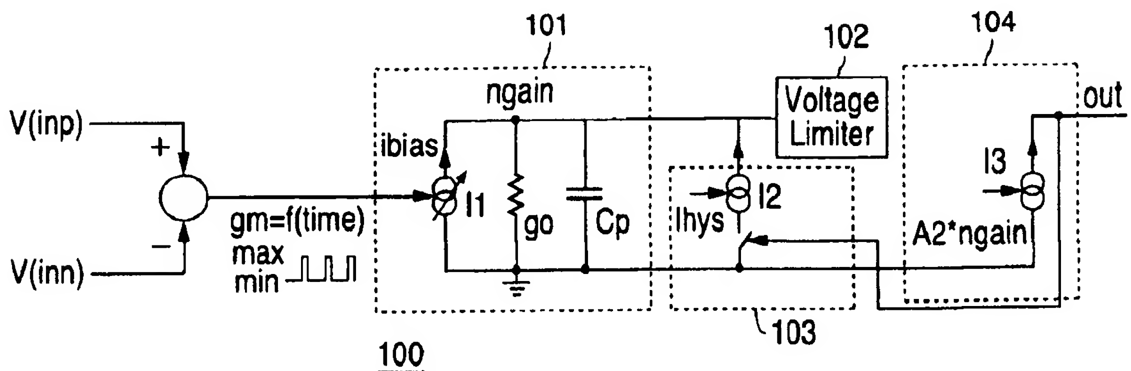
* cited by examiner

Primary Examiner—Tuan Lam

(57) **ABSTRACT**

A direct relationship exists between an integrated comparator's propagation delay and the input differential pair's bias current and overdrive voltage. A new method using a pulsed bias scheme for the input differential pair improves propagation delay by more than one order of magnitude without increasing significantly the average quiescent current, as long as the pulse width of the bias current is small relative to the system clock. A voltage limiter optimizes the comparator's transition time and a built-in hysteresis circuit minimizes spurious output transitions whenever the pulsed bias current pulse changes state. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.

20 Claims, 2 Drawing Sheets



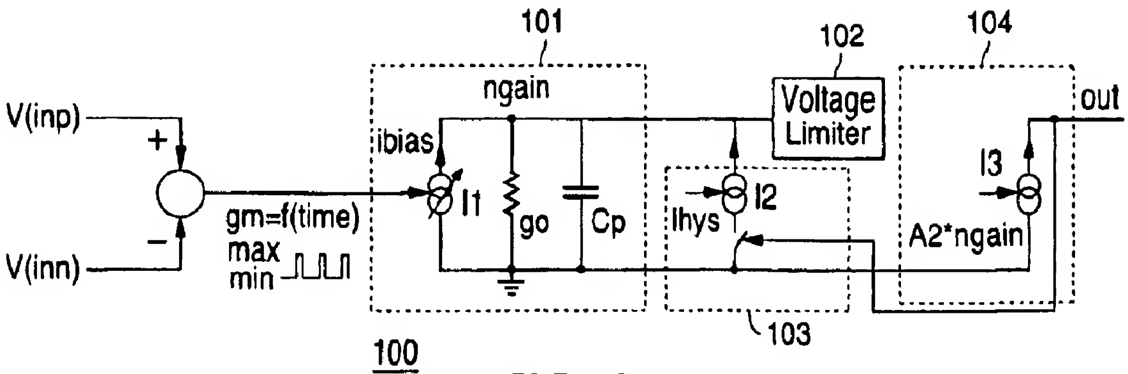


FIG. 1

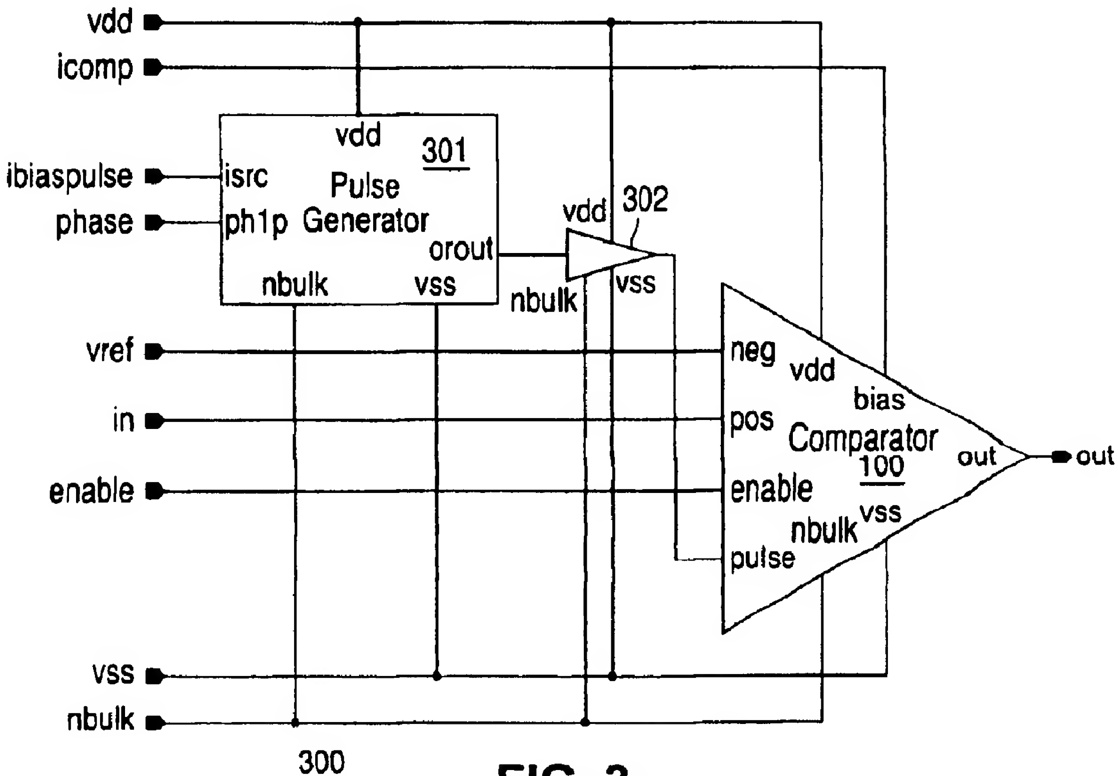


FIG. 3

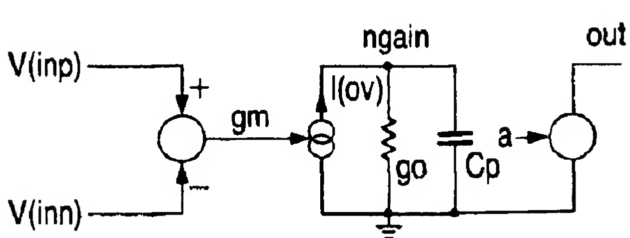


FIG. 4

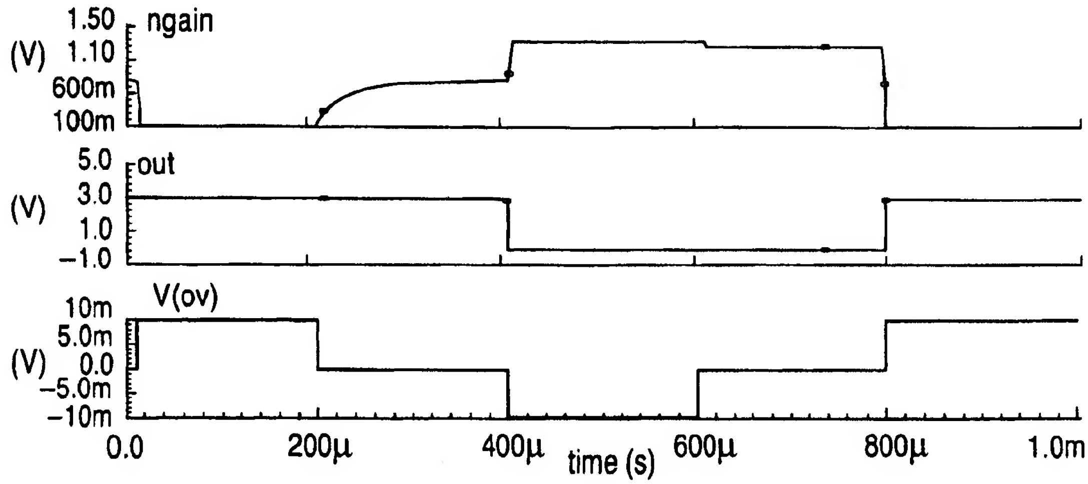


FIG. 2A

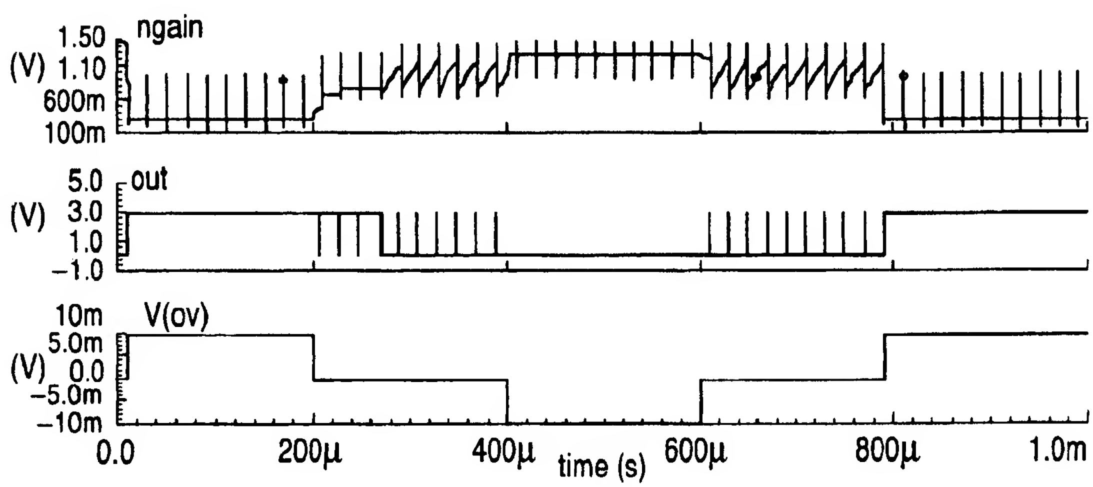


FIG. 2B

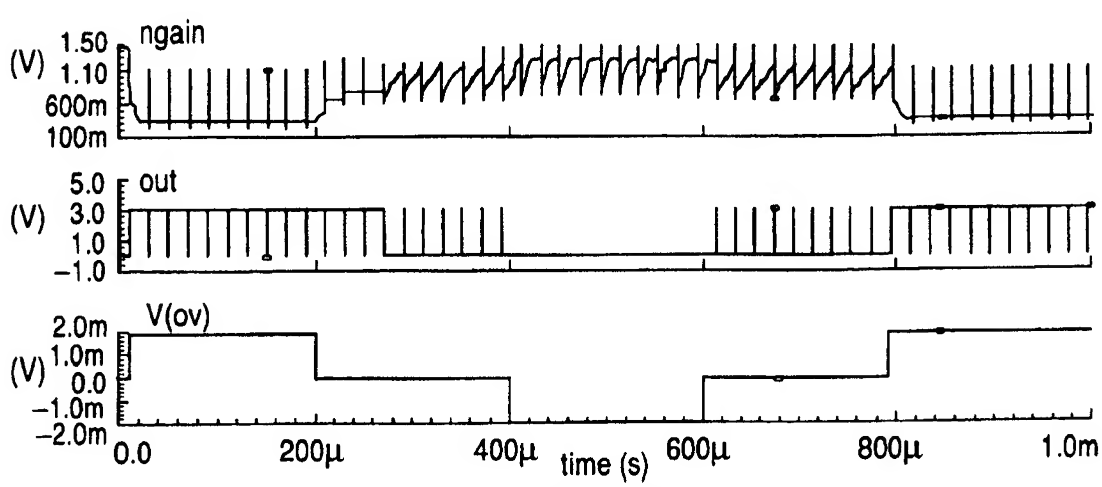


FIG. 2C